UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/758,228	01/16/2004	Si-Ty Lam	200313187-1	5728

22879 7590 07/13/2006

HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

EXAMINER	
KALAM, ABUL	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 07/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/758,228	LAM ET AL.	
	Examiner	Art Unit	
	Abul Kalam	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-49* is/are pending in the application.

4a) Of the above claim(s) *18-49* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/16/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Election/Restrictions

Applicant's election without traverse of Group I, Species I associated with claims 1-17, in the reply filed on May 1, 2006 is acknowledged. Thereby, claims 18-49 are withdrawn from further consideration.

Claim Objections

1. Claims 7-9 and 15-17 are objected to because of the following informalities:

The limitation, "a voltage supply," in line 2 of claims 7 and 15, has already been claimed in line 7 of claim 1, and because claims 7 and 15 depend from claim 1, there is an antecedent basis issue with the limitation. Is the voltage supply in claim 7 and 15 the same voltage supply as in claim 1? Claims 8 and 9 depend from 7, and claims 16 and 17 depend from claim 15, and thus these claims are also objected to.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 7-9 and 15-17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claims 7-9 and 15-17, the phrase "such as" in line 4 of claims 7 and 15, renders the claim indefinite because it is unclear whether the limitations following

the phrase are part of the claimed invention. See MPEP § 2173.05(d). Claims 8 and 9 depend from 7, and claims 16 and 17 depend from claim 15, and thus these claims are also rejected.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-4, 6, and 10-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Eguchi et al. (5,623,476).

With respect to claim 1, Eguchi teaches a data storage device (fig. 1) comprising:

a storage medium (1) comprising;

an electrode (103); and

an electrolyte layer (101) positioned on the electrode;

at least one probe (102) configured to contact the electrolyte layer, wherein the electrolyte layer is positioned between the probe and the electrode; and

a voltage supply device (108) configured to supply voltage through the at least one probe and the electrode to thereby create a circuit between the at least one probe and the electrode, wherein the level of voltage supplied by the at least one probe allows at least one of writing, reading, and erasing operations on one or more memory cells of the storage medium (col. 15, lns. 13-23; col. 18, lns. 53-67; col. 19, lns. 1-18).

With respect to claim 2, Eguchi teaches the device according to claim 1 as set forth above, wherein the electrode comprises one or more of gold, silver, copper, platinum, iridium, and palladium (col. 14, lns. 35-48).

With respect to claim 3, Eguchi teaches the device according to claim 1 as set forth above, wherein the electrolyte layer comprises a chalcogenide-metal composition (col. 13, lns. 41-55).

With respect to claim 4, Eguchi teaches the device according to claim 3 as set forth above, wherein the chalcogenide-metal composition comprises one or more of arsenic, germanium, selenium, sulfur, oxygen, tellurium, and antimony (col. 13, lns. 41-55).

With respect to claim 6, Eguchi teaches the device according to claim 3 as set forth above, wherein one or both of the storage medium and the at least one probe are movable with respect to each other (col. 18, lns. 59-65).

With respect to claim 10, Eguchi teaches the device according to claim 3 as set forth above, wherein the at least one probe comprises an inverted conical tip configured to contact the electrolyte layer (col. 14, lns. 55-63)

With respect to claim 11, Eguchi teaches the device according to claim 3 as set forth above, wherein the storage medium further comprises: a conductive layer positioned on the electrolyte layer, wherein the at least one probe is configured to contact the conductive layer (col. 14, lns. 49-54).

With respect to claim 12, Eguchi teaches the device according to claim 3 as set forth above, wherein the conductive material comprises one or more of gold, silver, copper, platinum, iridium, and palladium (col. 14, lns. 35-48).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 5, 7-9 and 13-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eguchi et al. ('476) as applied to claims 1, 3, and 11 above, and further in view of Moore et al. (US 2005/0122757).

With respect to claim 5, Eguchi teaches all the limitations of the claim, as set forth above in claims 1 and 3, with the exception of explicitly disclosing:

wherein the chalcogenide-metal composition comprises silver.

However, Moore teaches wherein the chalcogenide-metal composition comprises silver (pg. 1, [0006]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the chalcogenide-metal composition of Eguchi to include silver in the chalcogenide-metal composition, as taught by Moore, because this is well known in the art of manufacturing PCRAM structures.

With respect to claims 7-9, Eguchi teaches all the limitations of the claim, as set forth above in claim 1, with the exception of disclosing:

with respect to claim 7, a voltage supply device is configured to supply a first voltage to perform a write operation in one or more memory cells of the storage medium, said first voltage being sufficiently high to form a conductive path in the electrolyte layer at the locations of the one or more memory cells;

with respect to claim 8, the device of claim 7 wherein the voltage supply device is configured to supply a second voltage to perform an erase operation in one or more memory cells of the storage medium, said second voltage having a reverse bias as compared to the first voltage, wherein the second voltage is operable to render a less conductive path in the electrolyte layer at the locations of the one or more memory cells;

and with respect to claim 9, the device of claim 7 wherein the voltage supply device is configured to supply a third voltage to perform a read operation on one or more memory cells of the storage medium, wherein the third voltage is a lower voltage than the first voltage or the second voltage and is sufficiently weak to cause little modification of the memory cell, said device further comprising: a resistance measuring device configured to detect the resistance between the at least one probe and the electrode.

However, Moore discloses a memory cell device in which a voltage supply device is configured to supply a first voltage to perform a write operation in one or more memory cells (110) of the storage medium, said first voltage being sufficiently high to

form a conductive path in the electrolyte layer at the locations of the one or more memory cells (pg. 4, [0050]-[0051]).

More also teaches wherein the voltage supply device is configured to supply a second voltage to perform an erase operation in one or more memory cells of the storage medium, said second voltage having a reverse bias as compared to the first voltage, wherein the second voltage is operable to render a less conductive path in the electrolyte layer at the locations of the one or more memory cells (fig. 6; pg. 4, [0045]).

Furthermore, More teaches wherein the voltage supply device is configured to supply a third voltage to perform a read operation on one or more memory cells of the storage medium, wherein the third voltage is a lower voltage than the first voltage or the second voltage and is sufficiently weak to cause little modification of the memory cell (fig. 5; pg. 3, [0043]), said device further comprising:

a resistance measuring device configured to detect the resistance between the at least one probe and the electrode (pgs. 3-4, [0044]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the device of Eguchi with the teachings of Moore, to supply three different voltages to perform the read, write, and erase operations, thus forming non-volatile memory devices capable of high long-term data integrity, rapid writing and erasure of data, and rapid addressing and reading of stored data.

With respect to claim 13, Eguchi teaches all the limitations of the claim, as set forth above in claims 1 and 11, with the exception of explicitly disclosing:

wherein the conductive layer comprises a plurality of discrete conductive elements spaced apart from each other discontinuously, wherein the plurality of discrete conductive elements are associated with memory cells.

However, Moore teaches a data storage device (figs. 1, 10, and 11) composed of memory cells (110) wherein a conductive layer (114) is comprised of a plurality of discrete conductive elements spaced apart from each other discontinuously (fig. 11), wherein the plurality of conductive elements are associated with memory cells (pg. 4, [0050]-[0051]).

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the device of Eguchi with the teaching of Moore, to have the conductive layer comprised of plurality of conductive elements, which are associated with memory cells, for the purpose of using the memory cells in programmable conductive memory elements, thus improving power consumption and enhancing the operating speed of devices with the memory components (pg. 1, [0008]).

With respect to claim 14, Eguchi and Moore teach the device of claim 13 as set forth above, and Moore further teaches wherein the electrode (116) is sized and positioned to create an electric circuit with the plurality of discrete conductive elements (114) (pg. 3, [0042]; pg. 4, [0051]).

With respect to claim 15, Eguchi and Moore teach the device of claim 14, as set forth above, and Moore teaches the device further comprising:

a voltage supply device configured to supply a first voltage to perform a write operation at the locations of the discrete conductive elements, said first voltage being

sufficiently high to form a conductive path in the electrolyte layer at the locations of the one or more memory cells associated with the discrete conductive elements (fig. 4; pg. 3, [0040]-[0042]).

With respect to claim 16, Eguchi and Moore teach the device of claim 15, as set forth above, and Moore further teaches wherein the voltage supply device is configured to supply a second voltage to perform an erase operation at the locations of the discrete conductive elements, said second voltage having a reverse bias as compared to the first voltage, wherein the second voltage is operable to render less conductive in the electrolyte layer at the locations of the one or more memory cells associated with the discrete conductive elements (fig. 6; pg. 4, [0045]).

With respect to claim 17, Eguchi and Moore teach the device of claim 16, as set forth above, and Moore further teaches wherein the voltage supply device is configured to supply a third voltage to perform a read operation at the locations of the discrete conductive elements, wherein the third voltage is a lower voltage than the first voltage or the second voltage and is sufficiently weak to cause little modification of the memory cell (fig. 5; pg. 3, [0043]), said device further comprising:

a resistance measuring device configured to detect the resistance between the at least one probe and the electrode at the locations of the one or more memory cells associated with the discrete conductive elements, said resistance being lower in those memory cells (pgs. 3-4, [0044]).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Abul Kalam whose telephone number is 571-272-8346. The examiner can normally be reached on Monday - Friday, 9 AM - 5 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AK

ANH D. MAI
PRIMARY EXAMINER